

## Features

- Double Poly/Double Metal
- 1.7 $\mu\text{m}$  Poly and 2.1 $\mu\text{m}$  Metal I Pitch
- 5.5 Volts Maximum Operating Voltage
- Twin-tub process, on N-type wafers
- ProToDuction<sup>™</sup> Option for low cost prototypes

## Description

The 0.8 $\mu\text{m}$  process provides flexibility, speed and packing density needed in mixed signal designs. The overall design rules are compatible with most other 0.8 $\mu\text{m}$  processes making second sourcing easy.

## Technology Outline

- Twin-tub technology
- Drain Engineered Structure to Ensure Reliability against Hot-Carrier Injection
- Planarization with non-etch-back SOG Processes
- State-of-the-art Metal technology :Ti/TiN/Al/TiN sandwich
- Latchup Free Process on Non-Epi material achieved

## Process Parameters

Process Parameters	0.8 $\mu\text{m}$ 5volts	Units
Metal I pitch (width/space)	1.1/1.0	$\mu\text{m}$
Metal II pitch (width/space)	1.2/1.0	$\mu\text{m}$
Poly pitch (width/space)	0.8/0.9	$\mu\text{m}$
Contact	0.9 x 0.9	$\mu\text{m}$
Via	1.0 x 1.0	$\mu\text{m}$
Gate geometry	0.8	$\mu\text{m}$
P-well junction depth	2.0	$\mu\text{m}$
N+ junction depth	0.25	$\mu\text{m}$
P+ junction depth	0.30	$\mu\text{m}$
Gate oxide thickness	180	Å
Inter poly oxide thick.	320	Å

## MOSFET Electrical Parameters

Electrical Parameters	0.8 MICRON - 5 volts						Units	Conditions
	N Channel			P Channel				
	min.	typ.	max.	min.	typ.	max.		
Vt (50x0.8 $\mu\text{m}$ )	0.50	0.65	0.80	0.53	0.68	0.83	V	saturation
I <sub>ds</sub> (50x0.8 $\mu\text{m}$ )		380			176		$\mu\text{A}/\mu\text{m}$	V <sub>ds</sub> =V <sub>gs</sub> =5v
Gain $\beta$ (50x50 $\mu\text{m}$ )		92			33		$\mu\text{A}/\text{V}^2$	V <sub>ds</sub> =0.1v
Body Factor (50x50 $\mu\text{m}$ )		0.74			0.52		$\sqrt{v}$	
Bvdss (50x0.8 $\mu\text{m}$ )	9	12		9	12		V	I <sub>ds</sub> =1pA
Subthreshold Slope		89			96		mV/dec.	V <sub>ds</sub> =0.1v
Maximum Substrate Current (50x0.8 $\mu\text{m}$ )		1.4			n/a		$\mu\text{A}/\mu\text{m}$	V <sub>ds</sub> =5.5v V <sub>gs</sub> =2.7v
Field Threshold	9	20		9	22		V	I <sub>ds</sub> = 14 $\mu\text{A}/\text{sq}$
L Effective		TBD			TBD		$\mu\text{m}$	L drawn = 0.8 $\mu\text{m}$

## 0.8 Micron CMOS Process Family

### Capacitances (fF/ $\mu\text{m}^2$ )

	min.	typ.	max.
Inter-poly	0.88	1.06	1.27
Gate oxide	1.7	1.9	2.1
N+ Junction		0.32	
P+ Junction		0.64	

### Bipolar gain<sup>1</sup>

	min.	typ.	max.
NPN vertical		227	

<sup>1</sup>Test condition :  $V_{ce} = 5$  volts

### Resistances ( $\Omega/\text{sq.}$ )

	min	typ.	max.
Pwell		5500	
Pwell in Pfield	2000	2300	2600
N+	20	50	80
P+	80	110	140
Poly gate	26	37	48
Poly capacitor	75	100	125
Metal I		0.038	
Metal II		0.038	

Preliminary Data